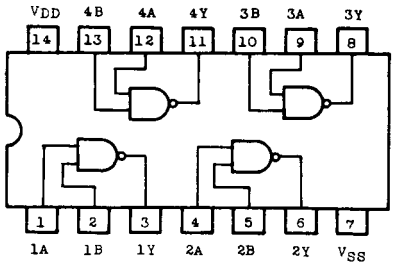
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

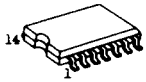
TC40H000P/F

TC40H000 QUAD 2-INPUT NAND GATE

PIN CONNECTION



DIP14(3D14A-P)



MFP14(F14GB-P)

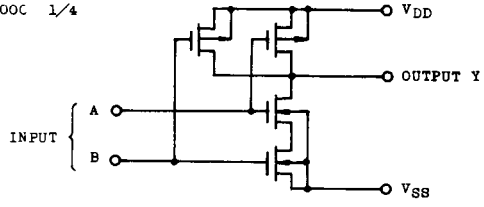
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+10$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

TRUTH TABLE

INPUT		OUTPUT
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

CIRCUIT DIAGRAM



* ALL INPUTS ARE EQUIPPED WITH PROTECTION CIRCUIT.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

TC40H000P/F

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

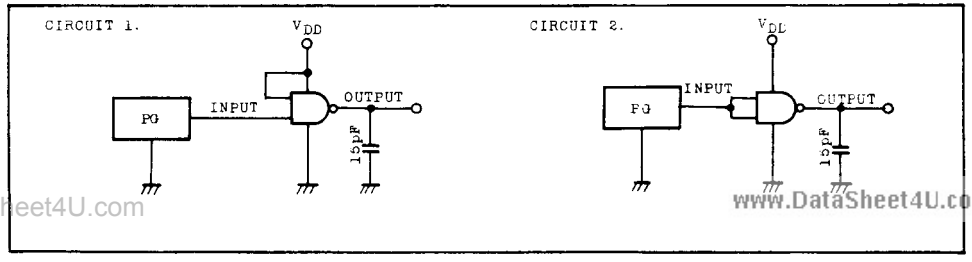
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS}$, V_{DD}	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
Input Voltage "H" Level	V_{IH}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V, 4.5V	5	4.0	-	4.0		-	4.0	-	V
Input Voltage "L" Level	V_{IL}		5	-	1.0	-		1.0	-	1.0	V
Input Current "H" Level	I_{IH}	V_{IH}=8.0V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	*$V_{IN}=V_{SS}$, V_{DD}	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations.

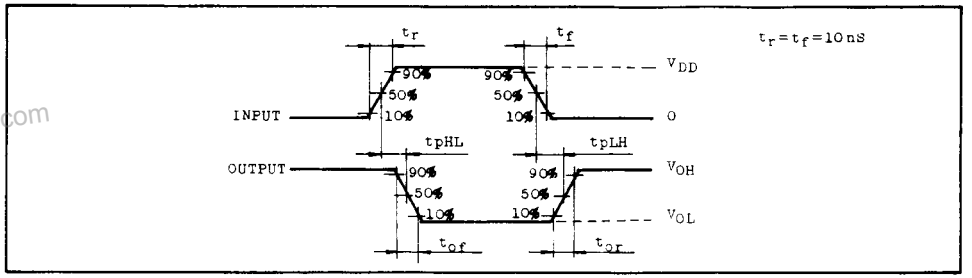
SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Circuit 1	5	-	26	40	ns
Output Fall Time		t_{of}	Circuit 1	5	-	16	30	ns
Propagation Delay Time	(Low-High)	t_{pLH}	Circuit 1	5	-	18	27	ns
	(High-Low)	t_{pHL}		5	-	14	21	
Propagation Delay Time	(Low-High)	t_{pLH}	Circuit 2	5	-	13	20	ns
	(High-Low)	t_{pHL}		5	-	15	23	
Input Capacitance		C_{IN}			-	5	-	pF

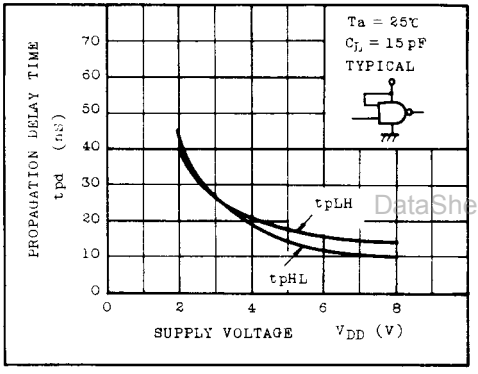
SWITCHING TIME TEST CIRCUIT



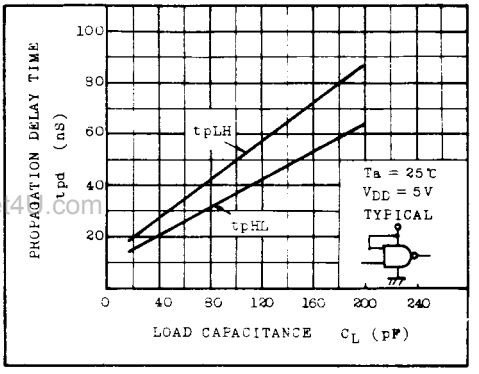
SWITCHING TIME TEST WAVEFORM



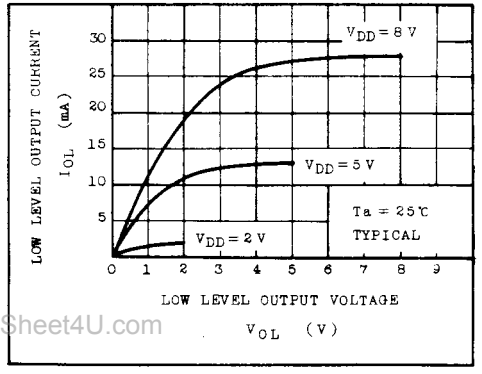
t_{pd} - V_{DD}



t_{pd} - C_L



I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})